

FIG. 2

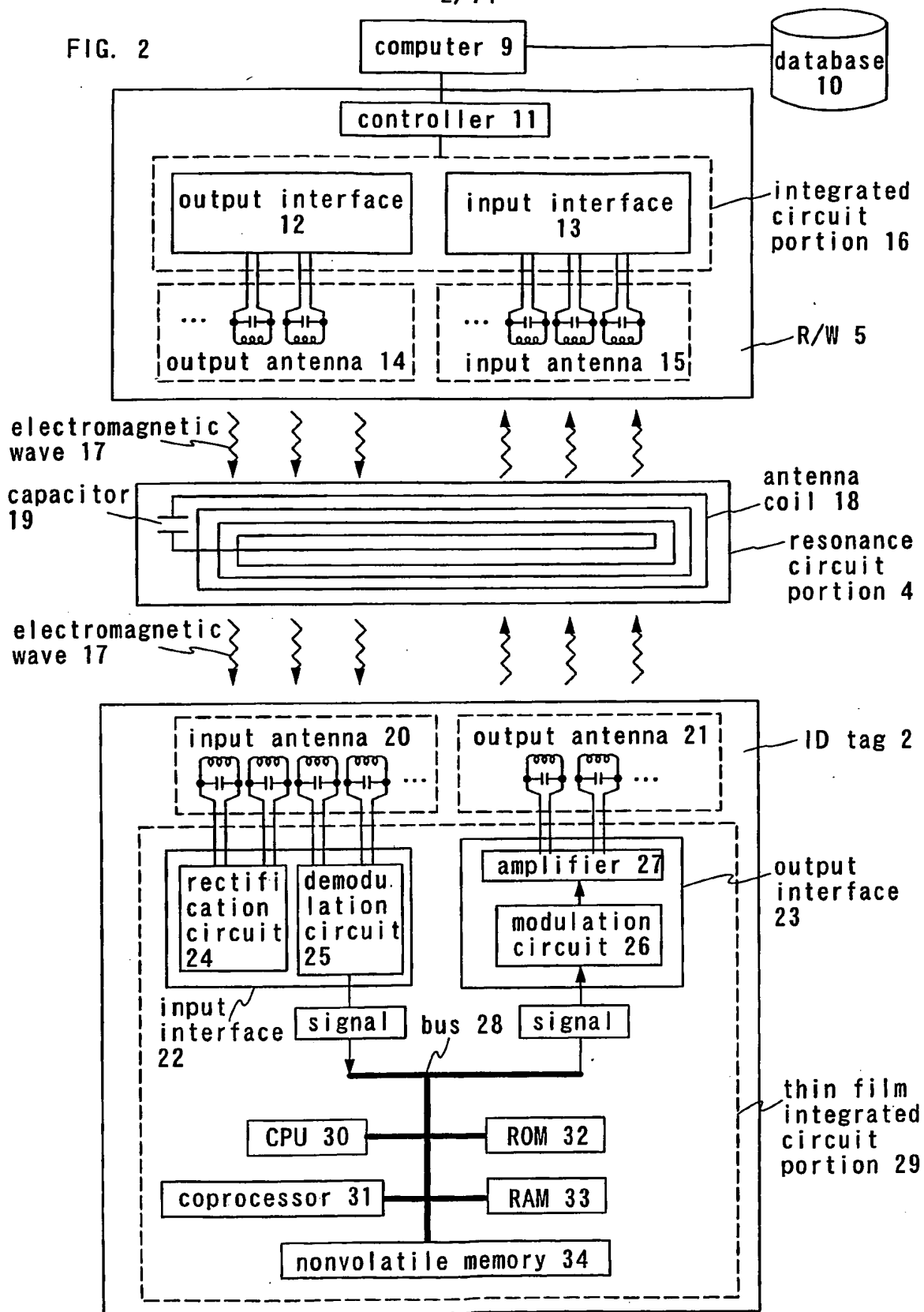


FIG. 3

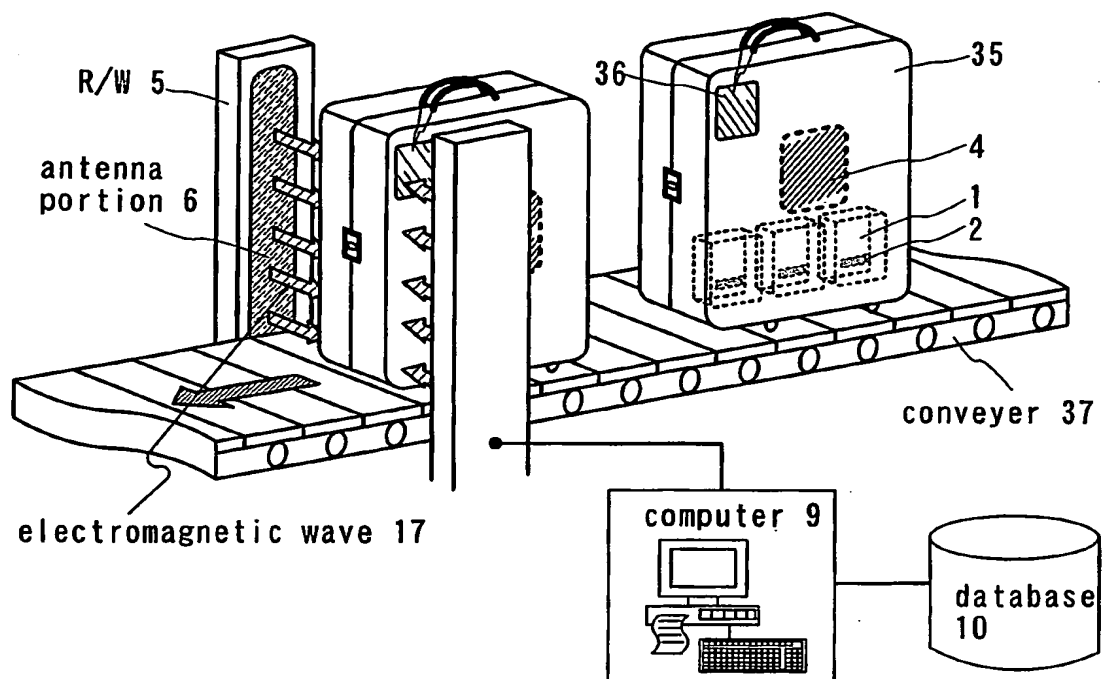
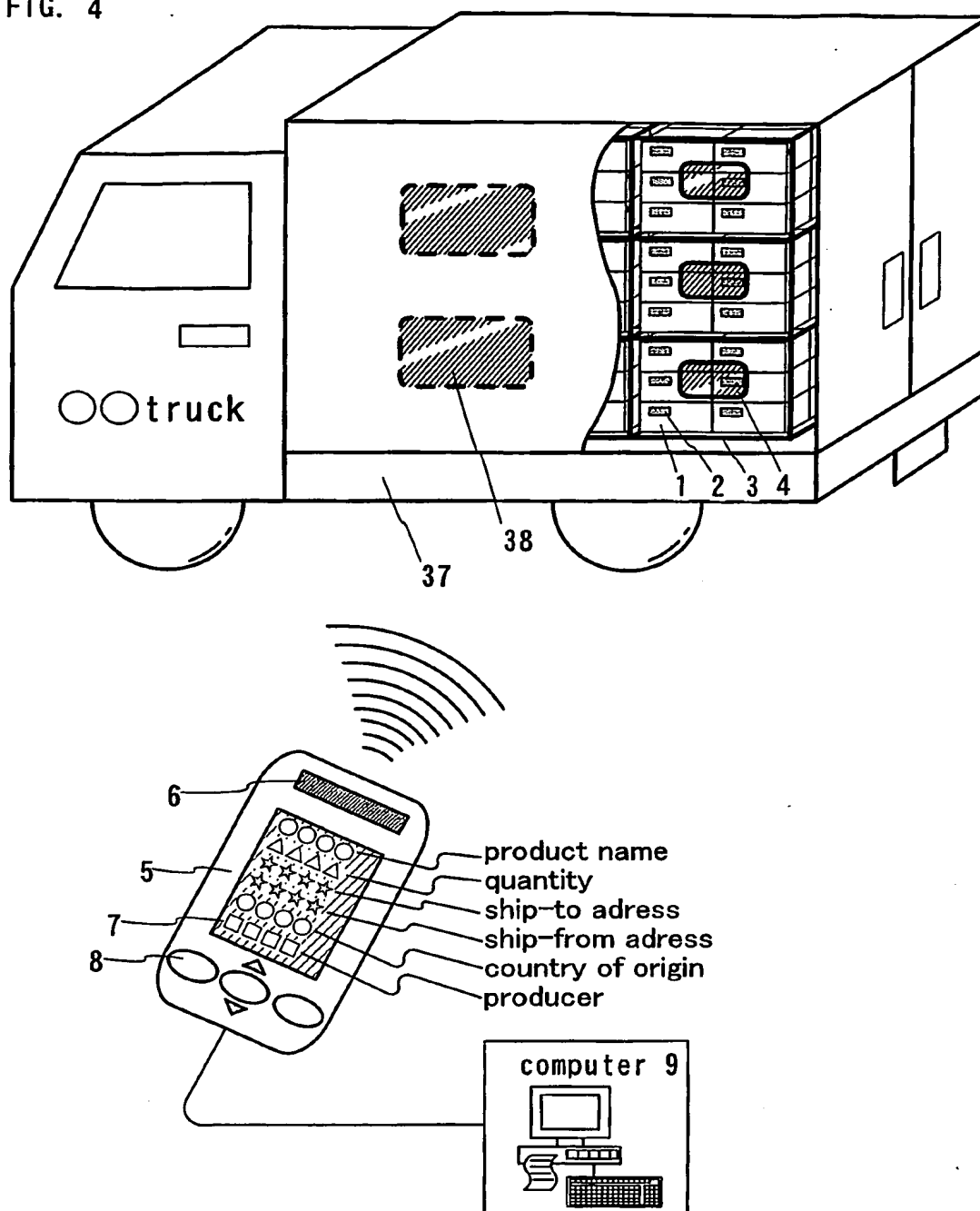


FIG. 4



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FIG. 5A

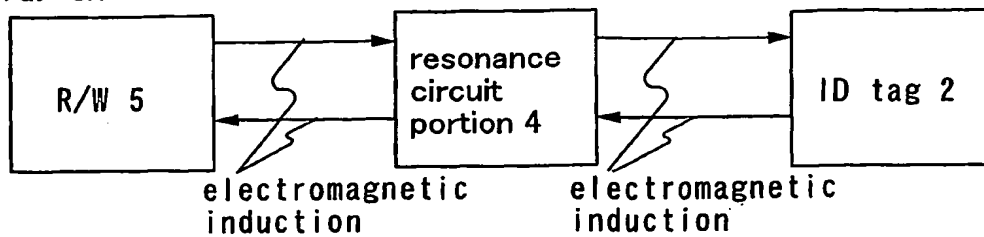


FIG. 5B

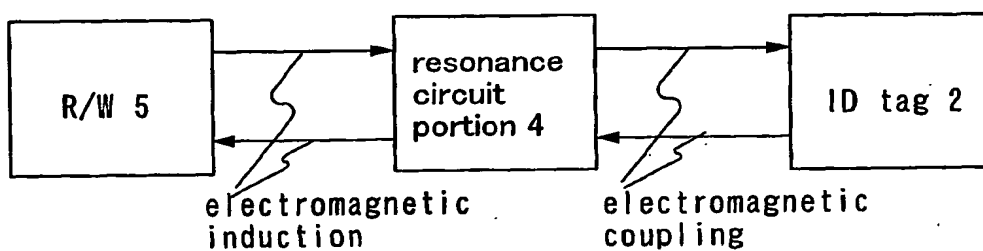
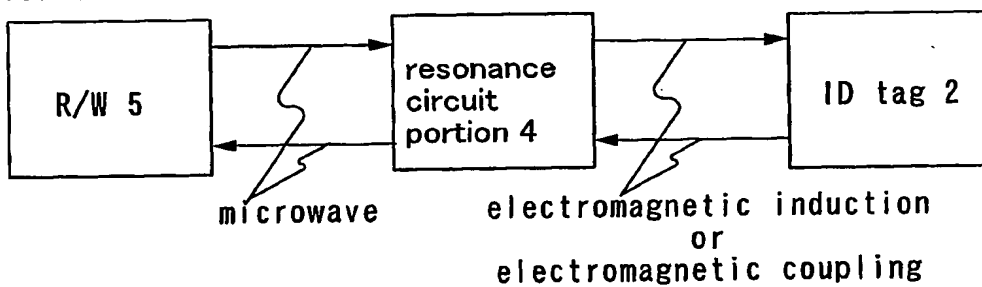


FIG. 5C



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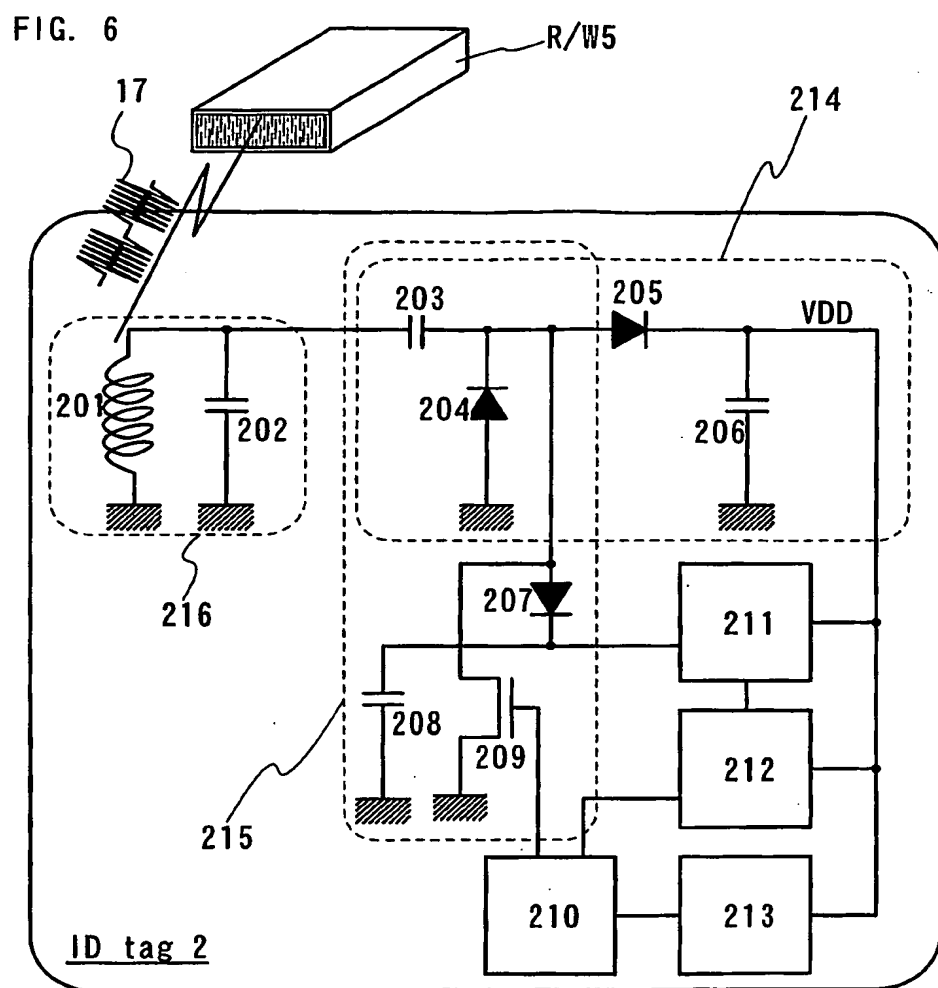


FIG. 7A forming separation layer and protective film

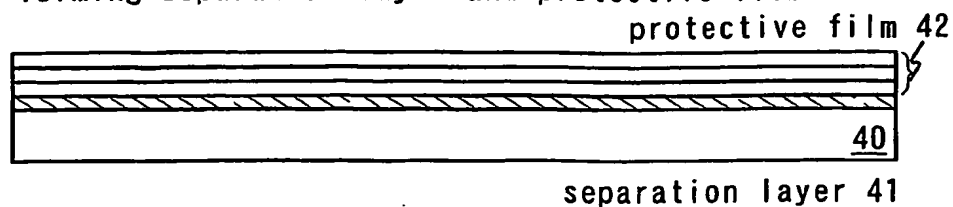


FIG. 7B forming semiconductor film and gate insulating film

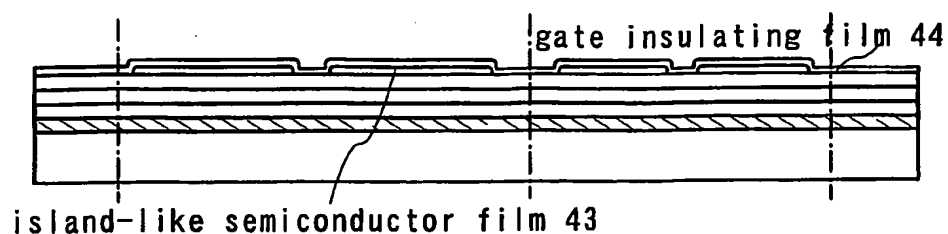


FIG. 7C forming gate electrode

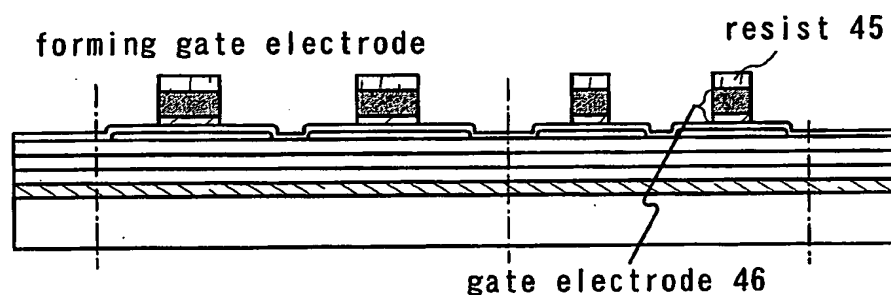


FIG. 7D forming n-type low concentration impurity region

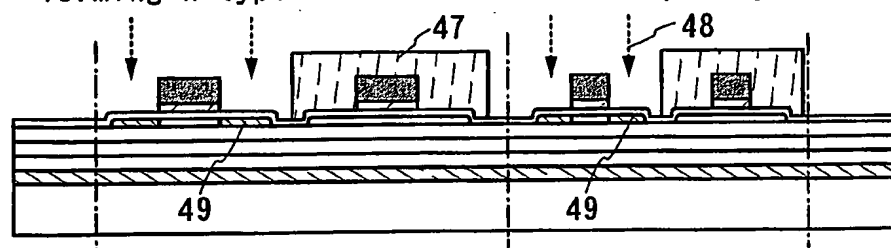


FIG. 7E forming p-type high concentration impurity region

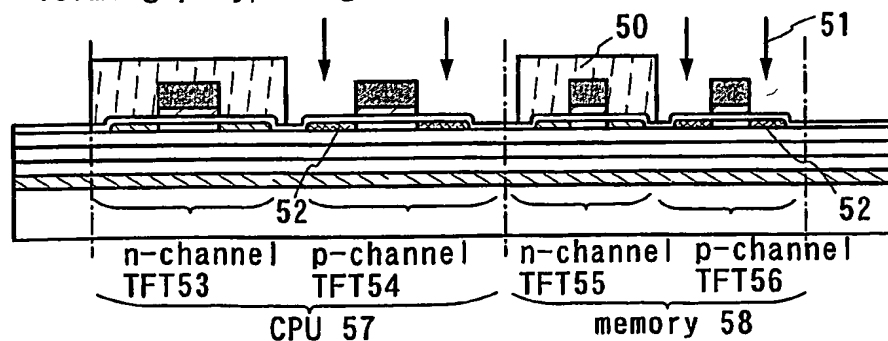


FIG. 8F forming insulatin film

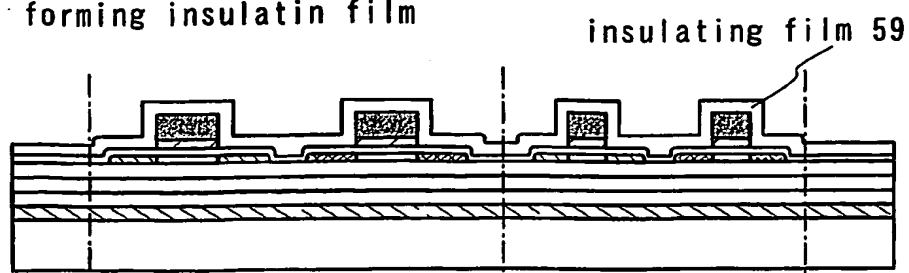


FIG. 8G etchback (forming sidewall)

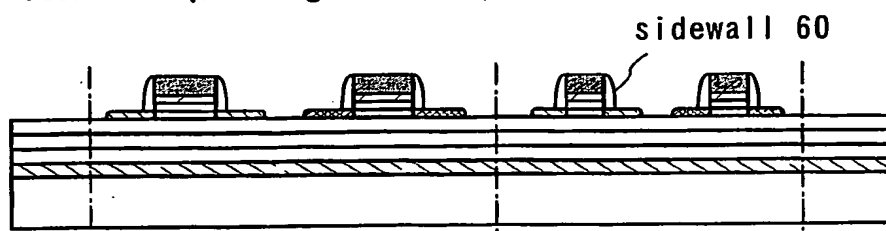
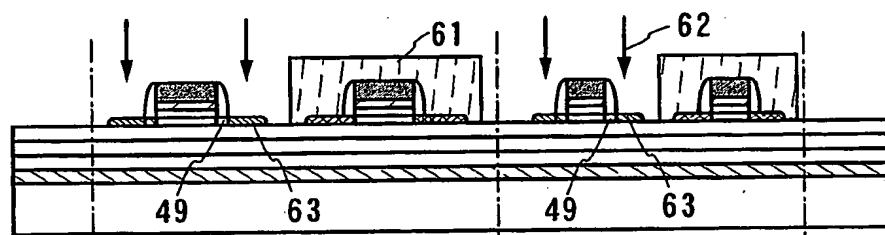


FIG. 8H forming n-type high concentration impurity region



**FIG. 81 forming interlayer, protective film and wiring**

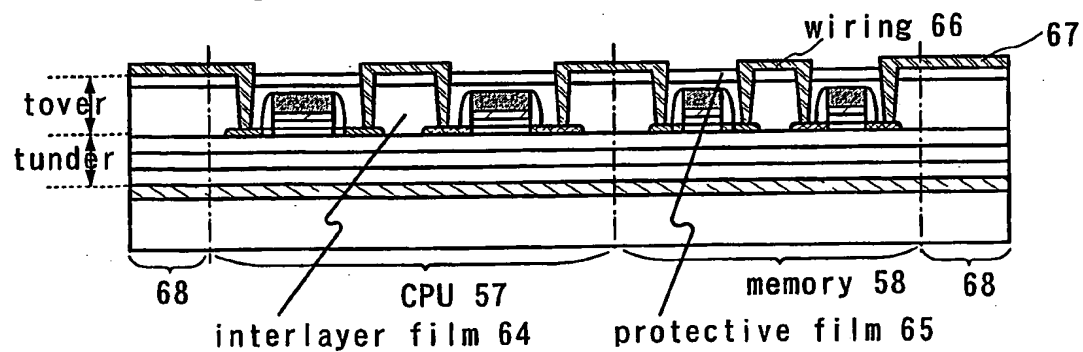




FIG. 9J forming thin film integrated circuit device

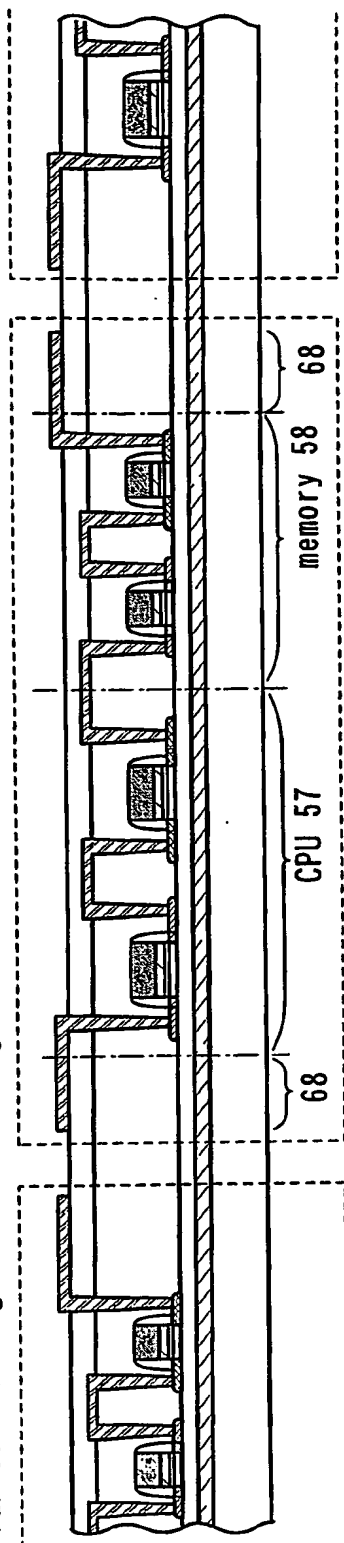


FIG. 9K forming groove

groove 70 thin film integrated circuit portion 69

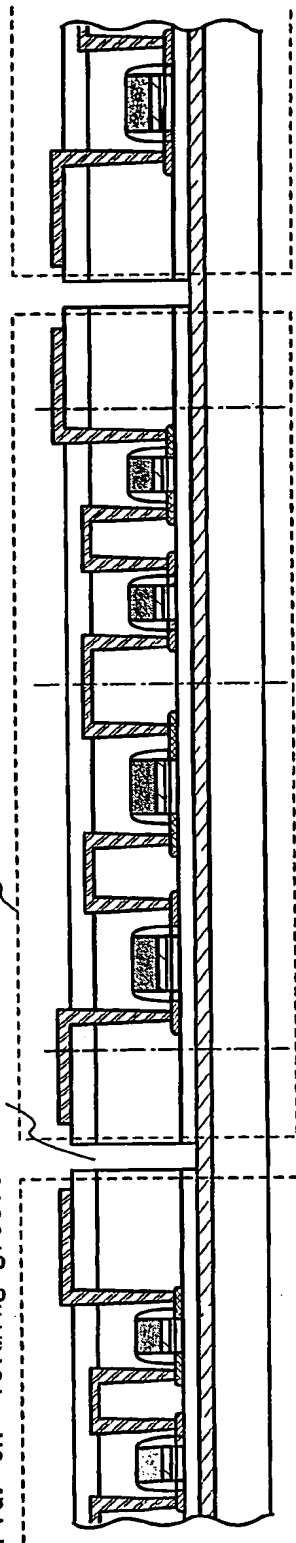


FIG. 9L attaching jig

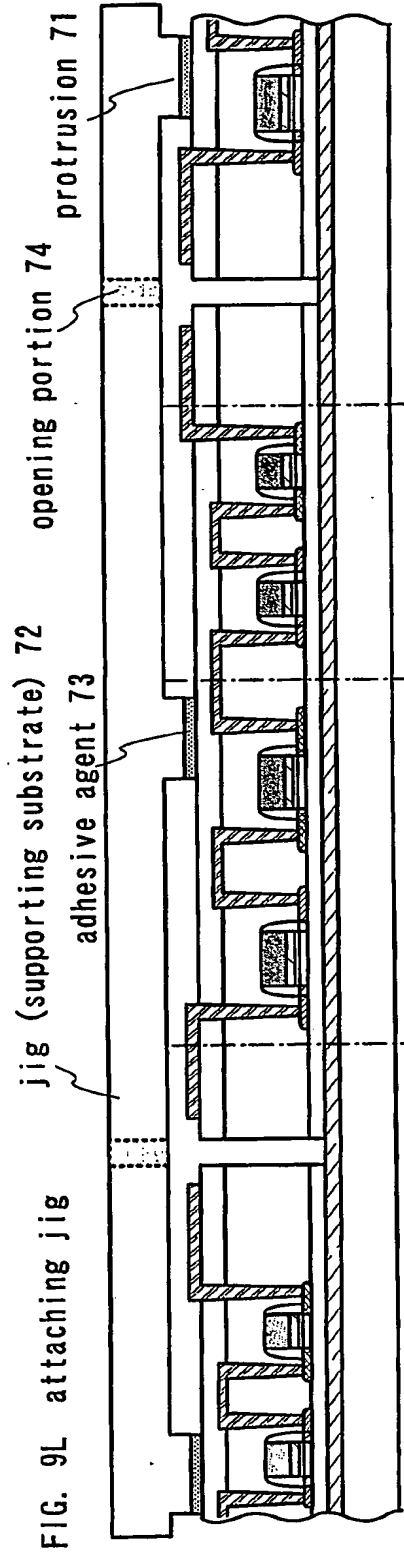


FIG. 10M introducing halogen fluoride

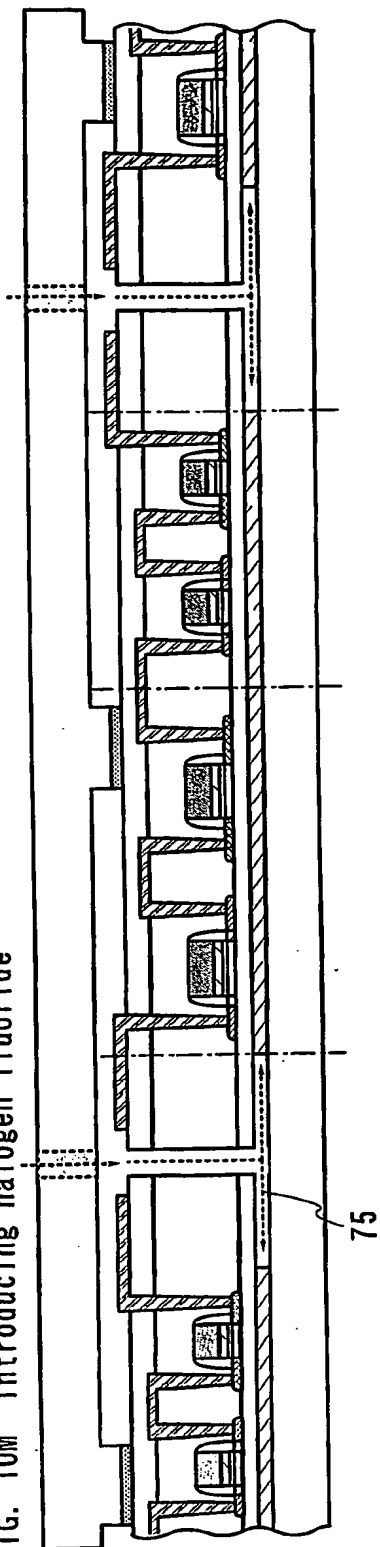


FIG. 10N separating substrate

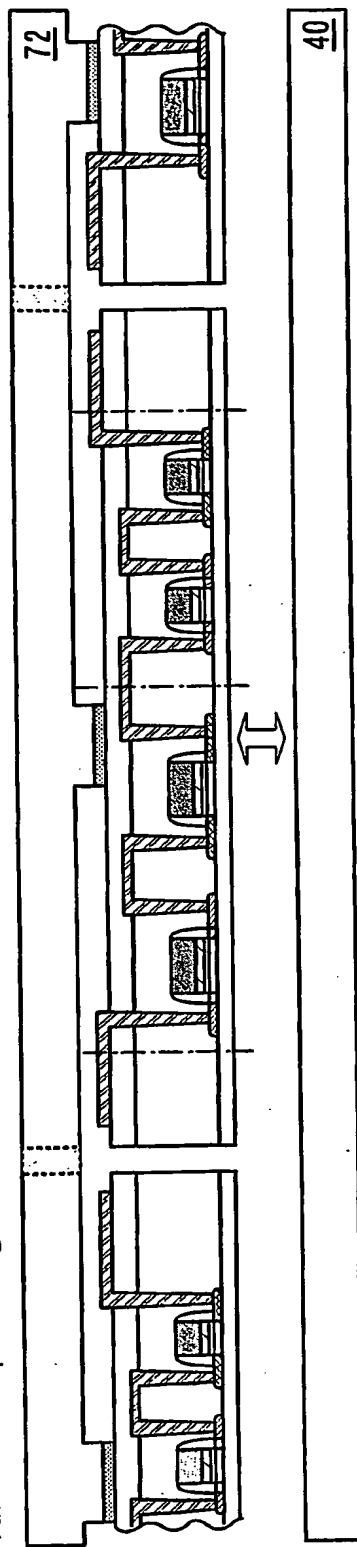
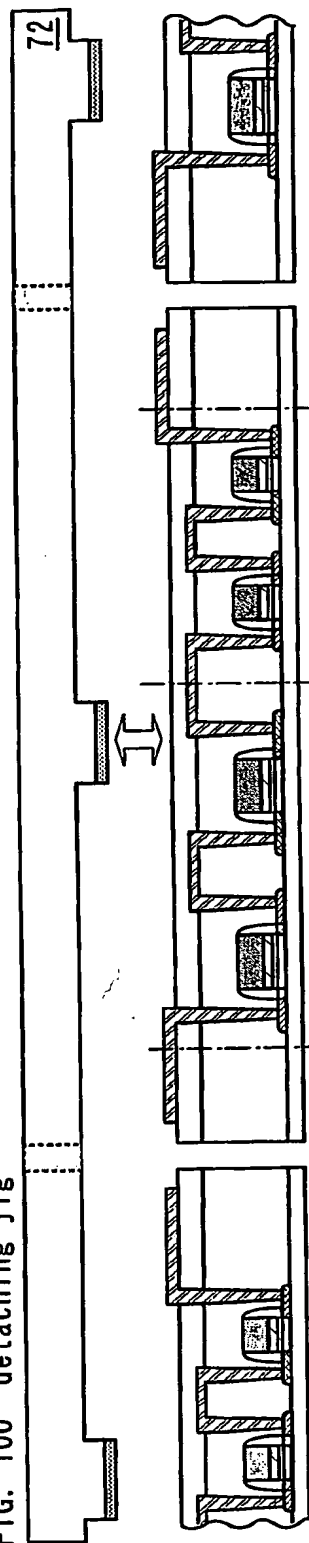


FIG. 100 detaching jig



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FIG. 11A

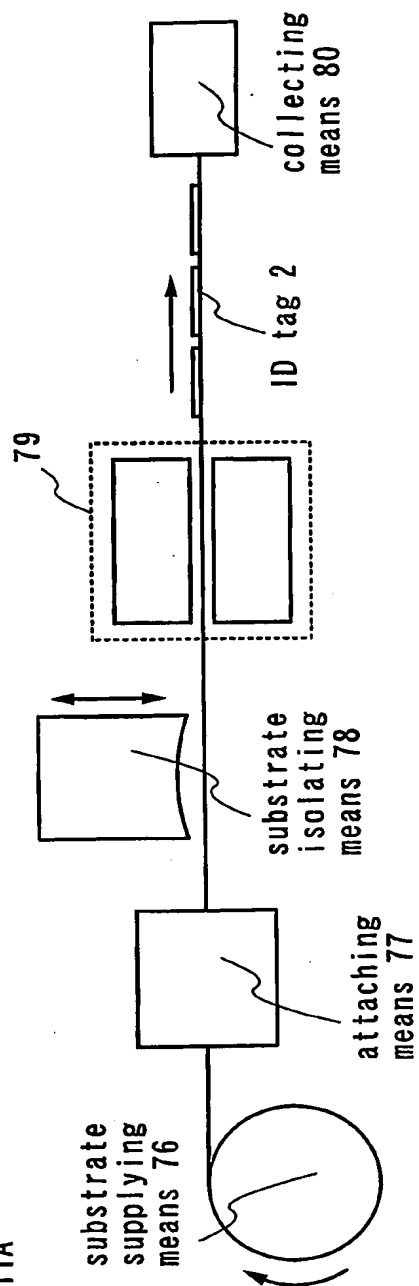
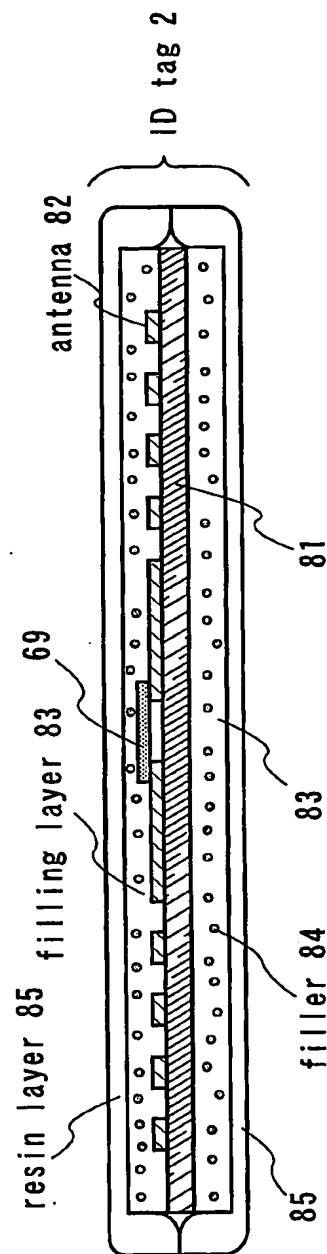


FIG. 11B magnified drawing of IDtag as a completed article



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FIG. 12

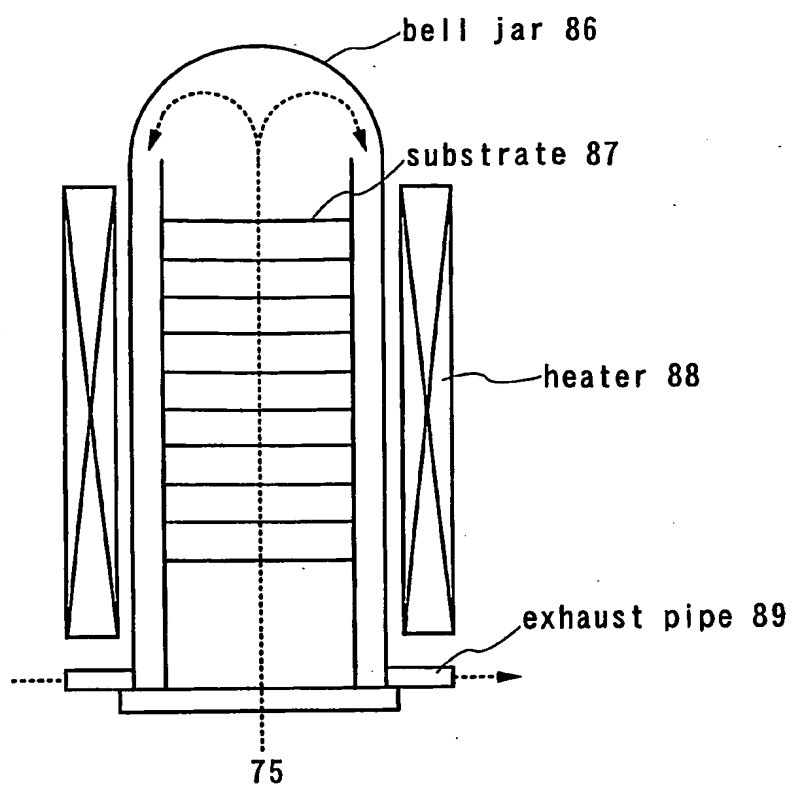


FIG. 13A transferring and aligning substrate

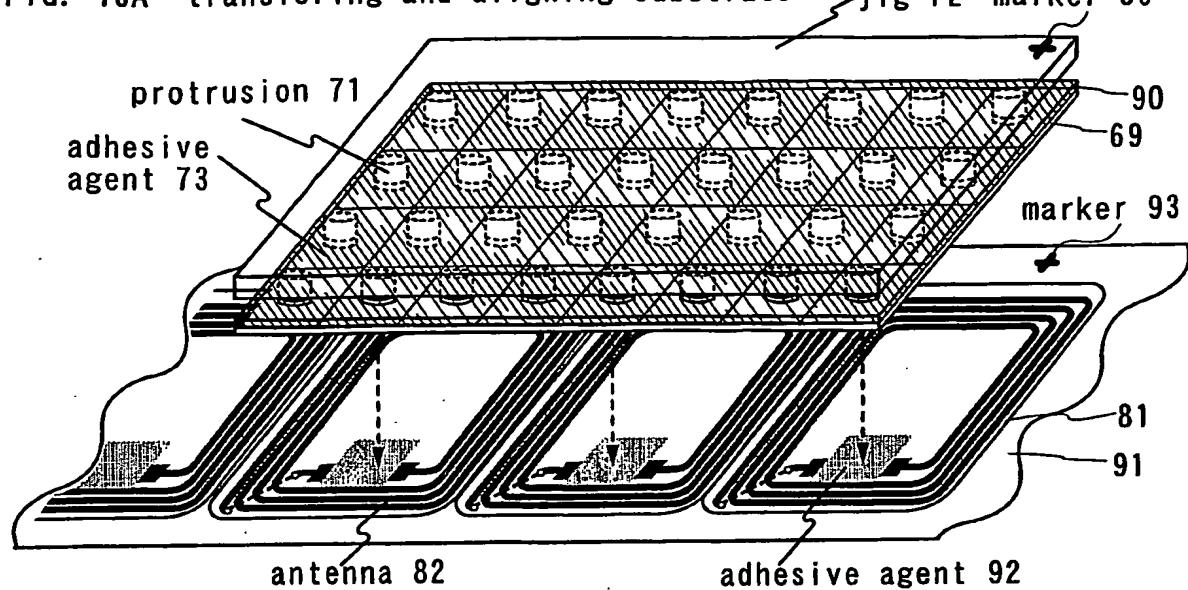


FIG. 13B attaching thin film integrated circuit portion

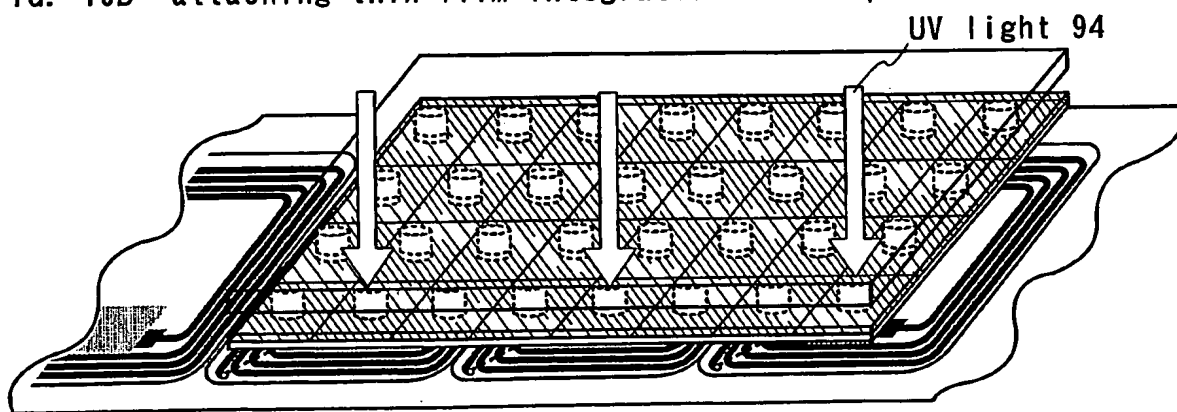


FIG. 13C covering by coating

